AMENDMENTS TO THE SPECIFICATION

Please amend page 1, line 3, of the application as filed (hereinafter "the application"), as follows:

Inventors: Ken Ostrom, Tim Ng, and Clifford Duong

Please add a new paragraph, starting at page 1, line 4 of the application as follows:

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Patent Application No. 60/229,657, filed on August 31, 2000, entitled "EFFICIENT SHUNT REGULATOR FOR TRANSIENT SUPPRESSION", and U.S. Provisional Patent Application No. 60/230,154, filed on September 1, 2000, entitled "METHODS AND APPARATUS FOR PROVIDING REGULATED POWER TO A MICROELECTRONIC DEVICE", and U.S. Provisional Patent Application No. 60/230,181, filed on September 1, 2000, entitled "MICROELECTRONIC POWER REGULATION SYSTEM AND METHODS OF FORMING AND USING THE SAME" and incorporates the disclosure of each such application by reference.

Please amend page 7, lines 4-9 of the application as follows:

A power regulation circuit 200 in accordance with another embodiment of the invention is illustrated in Figure 2. Circuit 200 includes a primary voltage regulator 210 (with optional feedback look 250) and a sense circuit 220, which are coupled to a power supply 230 and a load

240. Regulator 210, power supply 230, and load 240 may be configured and operate in a manner similar to regulator 110, supply 420-130, and load 140.

Please amend page 9, lines 10-14 of the application as follows:

FIG. 5 illustrates another circuit \$00 in accordance with another embodiment of the invention. The circuit Circuit 500 includes a primary voltage regulator 510 and a secondary voltage regulator 520, coupled to a power supply 505 and a load 550. Primary voltage regulator 510 converts an unregulated DC voltage to a regulated DC voltage (Vout), as described above in connection with primary regulators 110-410.

Please amend page 10, lines 12-23 of the application as follows:

In accordance with another aspect of the present embodiment, transistor 632 is suitably scaled in emitter area relative to the emitter area of transistor 634 such that the emitter area of transistor 632 is N times larger than that of transistor 634. For example, N can be scaled to a factor between 100 to 1000, or any other factor suitably configured to facilitate transistor 632 to be turned on essentially at all times of operation of system 600. The quiescent current of transistor 632 is approximately equal to N*fbias1 and is nominally independent of Vout supplied to load 550 by primary voltage regulator 610. In this manner, negative transient regulator 620 transistor 632 is always "on," allowing for rapid response to negative current transient events. To increase or maximize efficiency, the value of transistor 632 stand-by current (N*fbias1) is suitably chosen to be a small fraction of the transient current delivered by negative transient response portion 630 to load 550.

Please amend page 10, line 30 - page 11, line 2 of the application as follows:

The output current supplied by transistor 632 to load 550 is exponentially related to the dynamic change in transistor 632 base-emitter voltage. Voltage droop in power supply 600-505 under this dynamic condition can thus be reduced.

Please amend page 11, line 25 - page 12, line 4 of the application as follows:

As described above_with respect to transistor 632 of negative transient response portion 630, transistor 642 can be suitably scaled in emitter area relative to the emitter area of transistor 644, such that the emitter area of transistor 642 is K times larger than that of the area of transistor 644. For example, K can be scaled to a factor between 100 to 1000, or any other factor suitably configured to facilitate transistor 642 to be turned on essentially at all times. The quiescent current of transistor 642 is approximately equal to K*Ibias2 and is nominally independent of Vout supplied to load 550 by primary voltage regulator 610. In this manner, the positive transient response portion 640 transistor 642 is always "on," enabling rapid response to transient events. The value of transistor 642 stand-by current (K*Ibias2) is chosen to be a small fraction of the transient current delivered by transistor 642 to load 550 to increase efficiency.

Please amend page 12, lines 5-19 of the application as follows:

Dynamic variations in load voltage Vout, which are within the closed loop bandwidth of positive transient response portion 640, are tracked by amplifier 646, such that the current in

transistor 642 is held at the stand-by level, and regulation is performed by primary voltage regulator 610. Positive going dynamic variations in Vout due to a rapid decrease in the current demanded by the load that is beyond the bandwidth of amplifier 646 are regulated by transistor 642. Dynamic regulation is accomplished because the base voltage of transistor 642 established by amplifier 646 lags the transient variation of Vout under this condition. For transistor 642 comprising a bipolar transistor, the output current sourced by transistor 642 from the load is exponentially related to the dynamic change in transistor 642 base-emitter voltage, i.e.,

Lsub.E.congruent.k.sub.1e.sup.(Vbe/Vt), where k.sub.1 and Vt are constants, l.sub.E is the emitter current of transistor 642 and Vbe is the base-emitter voltage of transistor 642. Voltage peak in the power supply under this dynamic condition is thus reduced. The bandwidth of amplifier 642 646 is selected based on factors such as dynamic response of primary voltage regulator 610, secondary voltage regulator components, e.g., positive transient regulator 640, the desired degree of high frequency voltage regulation, and the efficiency of power delivery system 600.

Please amend page 16, lines 5-13 of the application as follows:

As the load current (I_Load) rapidly transitions from a high current (I_high) to a low current (I_low) beginning at time 14 at such a rate that primary voltage regulator 1 110 cannot immediately respond to the change in load current, the voltage at the load element (V_Load) rapidly transitions from a desirable nominal voltage (V_nom) to an undesirable voltage (V_nom+V_spike) as the dynamic load charge is momentarily absorbed by capacitive storage lo elements in close proximity to the load. Between time t5 and t6, the local capacitive storage

elements absorb the charge provided by the primary regulator that is no longer demanded by the load <u>1140</u>, resulting in an undesirable boost in the load voltage (V Load).

Please amend page 16, lines 18- page 17, line 8 of the application as follows:

Typical current waveforms of system 1100 in accordance with one embodiment of the invention are illustrated in Figure 13 and serve to further illustrate the operation of the improved regulation system. First, consider the condition whereby the load current (I Load) rapidly transitions from a low current state (I low) to a high current state (I high) beginning at time to at such a rate that primary voltage regulator 1110 cannot immediately source the demanded charge. Secondary regulator 1120 then responds at time t1 and rapidly provides the demanded increase in load current (e.g. using Boostl 1150 and circuit 1180) as shown by the I SR waveform of Figure 13. Secondary regulator 1120 is preferably designed in such a way as to minimize the time between t0 and t1. The rapid delivery of dynamic charge to the load by secondary regulator 1120 results in a significant improvement in the dynamic regulation accuracy of the voltage supplied to load 1140 (V. Load) such that the dynamic perturbation is reduced to V. nom-V. reg. where V_reg is << than V_spike of Figure 12. Secondary regulator 1120 continues to provide the demanded load current until such time that primary voltage regulator 1110 can respond which begins at time t2 thereby maintaining the desired nominal load voltage (V_nom). In accordance with the illustrated embodiment, during the transition period between time (2 and t3. secondary regulator 1120 output current response is designed to approximately inversely match the response of primary voltage regulator 1110 (I PR) for maximum regulation accuracy i.e. the sum of the current provided by primary regulator 1110 (I_PR) and secondary regulator 1120

(I_SR) approximately equals load element 1140 current (I_Load). Overall efficiency is maximized when secondary regulator +1120 output current hold time (t2-t1) and transition time (t3-t2) is minimized.

Please amend page 19, line 23-page 20 line 10 of the application as follows: Secondary regulator 1520 also contains a sense amplifier 1536, a boost transistor 1538, diodes 4540 1541 and 1542, a controlled current source 1543 having an output current of Iboost1, and a circuit 1544 to control the current source. Initially, Iboost1 is zero, diodes 4540 1541 and 1542 are not conducting current, and transistor 1538 is reversed biased and not conducting current. Sense amplifier 1536 sense at a load point 1546 and produces an output signal whose magnitude is in proportion to or otherwise related to the rate of change of the load current, thereby allowing secondary regulator 1520 to distinguish between load transient events that can be regulated by primary voltage regulator 1510 and transient events that require secondary regulator 1520 to respond for maximum overall system 1500 regulation effectiveness and efficiency. For low to high current load transients, circuit 1544 translates sense amplifier 1536 output into a signal suitable for control of source 1543 which is modulated from a zero or near zero state to an active or "on" state. In response to the current from source 1543, diodes 4540-1541 and 1542 conduct current, transistor 1538 is forward biased and conducting current, and transistor 1522 conducts current in proportion to Iboost1 and the emitter area ratio of transistor 1538, diode-1540 1541 and 1542 and transistor 1522. Transistor 1522 then becomes an active charge-sourcing element and responds to satisfy the demand in load current. Charge is then quickly transferred from a secondary output voltage node 1115 to primary voltage node

1550. Operation of the circuit in terms of current profiles is similar to that illustrated in Figure 13.

Please amend page 20, lines 28-30 of the application as follows:

An additional embodiment of the invention is illustrated in FIG. 16. In addition to the elements of FIG. 15, the embodiment of FIG. 16 adds diodes 1602 and 1604 and a resistor 1606 having a resistance value of R4.

Please amend page 22, lines 4-14 of the application as follows:

A system 1900 in accordance with another exemplary embodiment is illustrated in Figure 19. System 1900 is similar to system 1800. Operation of the low to high low transient circuitry as system 1900 is as follows. Initially, alboost1 is zero, diodes 1902 and 1904 and transistor 1908 are "off." Transistor 1906 and diode 1910 are biased solely by Ibias1. Transistors 1906 and diode 1910 are scaled in emitter area such that along with resistor 4942 the quiescent current of transistor 1906 is approximately equal to n*Ibias1 (where n>>1) and is nominally independent of the voltage supplied to the load by regulator 1510. For high to low current load transients, a circuit 1912 translates a sense amplifier 1536 output into a signal suitable for control Iboost1 which is modulated from a zero or near zero state to an active or "on" state. Transistor 1908 and diodes 1902 and 1904 then drive transistor 1906 to conduct current in proportion to n times Iboost1.

Application No. 09/945,187 Response to Notice of Allowance Submitted 20 February 2008

Please amend page 22, lines 24-28 of the application as follows:

A system 2000 in accordance with another exemplary embodiment is illustrated in Figure 20. System 2000 is similar to system 1900, except system 2000 includes a tertiary output voltage 2005 supplied to transistor 2002 from a primary voltage regulator 2010 which voltage can be a lower potential than the secondary voltage provided by primary voltage regulator 1510-2010. The tertiary output voltage allows further optimization of the efficiency of a secondary regulator 2020.

[REMAINDER OF THIS PAGE INTENTIONALLY LEFT BLANK]